Patent
Attorney's Docket No. 032840-003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT
APPLICATION TRANSMITTAL LETTER

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed for filing is the utility patent application of Ted JOHANSSON, Arne RYDIN and Christian NYSTRÖM for SEMICONDUCTOR DEVICE WITH DEEP SUBSTRATE CONTACTS.

Also enclosed are:

[X] 4 sheet(s) of [X] formal [ ] informal drawing(s);

[X] a claim for foreign priority under 35 U.S.C. §§ 119 and/or 365 is [ ] hereby made to _ filed in _ on _;
[X] in the declaration;

[ ] a certified copy of the priority document;

[ ] a General Authorization for Petitions for Extensions of Time and Payment of Fees;

[ ] _____ statement(s) claiming small entity status;

[ ] an Assignment document;

[ ] an Information Disclosure Statement; and

[ ] Other: _____.

[X] An [ ] executed [X] unexecuted declaration of the inventor(s)
[X] also is enclosed [ ] will follow.

[X] Please amend the specification by inserting before the first line the sentence --This application claims priority under 35 U.S.C. §§119 and/or 365 to 9900446-7 filed in Sweden on February 10, 1999; the entire content of which is hereby incorporated by reference.--

[ ] A bibliographic data entry sheet is enclosed.

21839

(12/99)

[X] The filing fee has been calculated as follows [ ] and in accordance with the enclosed preliminary amendment:

CLAIMS					
	NO. OF CLAIMS		**EXTRA CLAIMS**	**RATE**	**FEE**
Basic Application Fee					$690.00 (101)
Total Claims	10	MINUS 20 =	-0-	x $18.00 (103)	-0-
Independent Claims	1	MINUS 3 =	-0-	x $78.00 (102)	-0-
If multiple dependent claims are presented, add $260.00 (104)					---
Total Application Fee					690.00
If verified Statement claiming small entity status is enclosed, subtract 50% of Total Application Fee					---
Add Assignment Recording Fee of if Assignment document is enclosed					-0-
TOTAL APPLICATION FEE DUE					**690.00**

[ ] This application is being filed without a filing fee. Issuance of a Notice to File Missing Parts of Application is respectfully requested.

[X] A check in the amount of $ 690.00 is enclosed for the fee due.

[ ] Charge $ _____ to Deposit Account No. 02-4800 for the fee due.

[X] The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17 and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in duplicate.

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Semiconductor device with deep substrate contacts

Technical field of the invention

The present invention relates to a semiconductor device and to a semiconductor integrated circuit mounted in a package comprising a semiconductor circuit with at least one semiconductor device.

Description of related art

An operating frequency for modern telecommunication electronics range from several hundred megahertz up into the gigahertz region. Power transistors operate most efficiently at large signal levels and high current densities. Present high-voltage silicon RF power transistors can deliver several hundreds of Watts of output power at frequencies greater than 2 GHz and are operated at typically 25 V. These transistors are typically used in stationary applications, like output amplifiers in cellular base stations, digital broadcasting, or television transmitters.

For applications like wireless handy phones, the supply voltage is limited to 2-6 V range (battery operation), the output power is in the 0.1-4 W range and the operating frequency is in the 1-3 GHz range.

The dominating type of technology in this field is GaAs-based, but silicon-based circuits are now being developed in this area. Silicon's main advantage is the considerably lower price, and its disadvantage the more limited performance at high frequencies.

A common difficulty for all RF power applications is to maintain the power gain and output power when the operating frequency is increased and the supply voltage is decreased. Especially a parasitic emitter/source inductance from bonding wires is deleterious for this performance, because it

constitutes a critical part of transferring power to a load. This will ultimately lead to a limitation in the size of the devices and the usefulness of the devices for a certain application. This applies as well for integrated amplifiers with lower voltage and lower power as for discrete high voltage RF power transistors, in bipolar and MOS technologies. A low impedance connection to ground is essential for these types of devices.

An integrated circuit, comprising a plurality of semiconductor devices, manufactured on a semiconductor substrate, is normally placed in a package with pins or other means to contact the integrated circuit. The pins are normally connected to the integrated circuit via bonding wires, which can have different length. A ground pin may be connected to a lead-frame, so called fused lead-frame, on which the integrated circuit is mounted, where the reverse side of the substrate is in electrical contact with the lead-frame.

A normal connection from bond pads on the integrated circuit to the pins is obtained via long bonding wires, having approximately 1nH/mm in inductance and approximately 3mΩ/mm in resistance at DC for a bonding wire with a diameter of 10-30 µm (1-2 mils). Parallel bonding wires are used to minimise the inductance and the resistance.

A typical length of a bond wire in a package is 1-2 mm, which gives an inductance of 1-2 nH/bond wire. By introducing short bonding wires from bond pads down to the lead-frame for the ground connection, the inductance may be reduced down to 0.2 nH, which creates an impedance of approx. 2.5 Ohms at 2 GHz.

Existing techniques used to create low impedance contacts between the source and the substrate in a Lateral DMOS transistor comprises high doped diffused plugs or contact

structures including a trench filled with a conductor as is described in US patent 5,821,144 by D'Anna et al.

Other types of contacts creating a low impedance contact have etched holes through the substrate, which are filled with metal, for GaAs MESFET applications.

Deep tungsten filled substrate contacts for semiconductor devices with high frequency applications are described in the patent application WO 97/35344, by Norström et al. The contacts provide a direct ccupling means between a first metal layer and a highly doped substrate through a low doped epitaxial layer, in which said devices are implemented. The patent application comprises a method and a device for use as an earth plane, interference and cross-talk reduction and screening.

Summary of the invention

An object of the present invention is to provide a semiconductor device having a ground connection, where said ground connection is arranged to be connected to a ground pin on a package via a low impedance connection, especially at high frequencies.

Another object of the present invention is to provide an integrated circuit, comprising a semiconductor circuit with at least one semiconductor device, mounted in a package, having a low impedance connection between a ground connection of said devices and a ground pin on said package.

These objects are achieved by a semiconductor device, which is arranged at a surface of a semiconductor substrate, having an initial doping, said device comprising an electrical connection, comprising at least one plug made of a material with a high conductivity, between said initially doped substrate and said surface of the substrate, and said device having at least one ground connection arranged to be connected

to a ground pin on a package, said at least one ground connection is arranged to be connected to said ground pin using said electrical connection, where said substrate is arranged to be connected to said ground pin via a reverse side of the substrate, opposite said surface, and thereby being arranged to establish a connection between said ground connection and said ground pin.

An advantage with the present invention is that a contact with low impedance may be established between a ground connection of a device and a ground pin on a package, especially for high frequency application.

Another advantage is that less bonding pads are needed on the surface of the semiconductor substrate for connecting a semiconductor device since the ground connection is connected via the reverse side of the substrate.

A further advantage is that bonding wires for a circuit, according to the present invention, is faster to connect in a package, since less bonding pads are needed.

Yet another advantage of the present invention is that a large amount of current may be directed through the ground connection by having a plurality of plugs for each ground connection.

Still another advantage is that any type of device with a ground connection easily may be connected through at least one plug without having to establish a conductive pattern to a bonding pad on an integrated circuit having at least one semiconductor device according to the invention.

The present invention will now be described with reference to the accompanying drawings.

Brief description of drawings

Fig. 1 shows a partial cross section of a semiconductor circuit, comprising a double polysilicon self-aligned bipolar transistor with a ground connection according to the present invention.

Fig. 2a-2e shows manufacturing steps for the semiconductor device and the electrical connection in Fig. 1.

Fig. 3 shows a perspective view of an integrated circuit mounted in a package with a semiconductor circuit having a ground connection connected to a ground pin according to the invention.

Detailed description of preferred embodiments.

Fig. 1 shows a partial cross section semiconductor circuit, comprising at least one double polysilicon self-aligned bipolar transistor 100 with an electrical connection 101 according to the present invention.

The semiconductor device 100, in this example a bipolar NPN transistor, is manufactured on a substrate 102, having an initial high doping of a first type p+, on which a first epitaxial layer is grown to form a buried layer 103, having a high doping of a second type n+ opposite said first type p+. A second epitaxial layer is grown on top of the buried layer 103 to form a n-well 104, where the second epitaxial layer has a doping of the second type n. The buried layer 103 and the n-well 104 jointly represents a collector region of the bipolar transistor 100.

The semiconductor device region is delimited by isolation means 105 stretching from the surface 106 of the substrate down under the buried layer 103 into the initially doped substrate. A field oxide 107 covers the surface of the substrate having a first opening for a collector C and a second opening for an

emitter E and a double base B. A highly doped region 108, of a doping of the second type n+, stretches from the surface of the first opening down to the buried layer 103, as is usual in this type of semiconductor device. The collector C is connected to the highly doped region 108 via a conductor 110 with a high conductivity, such as tungsten, a metal contact 111 and a doped polysilicon layer 125.

A thin region 109 is created at the surface in the second opening, having a doping of the first type p, representing a base region. Three separate regions 112, 113 are created at the surface of this region 109. A highly doped region with a doping of a second type n+ is created in the centre, forming an emitter region 112. The emitter region is connected to a doped polysilicon layer 114, which in turn is connected to the emitter E via a metal contact 115 and a connector 116 with a high conductivity.

A base contact region 113 is created on each side of the emitter region 112, to which each base B is connected via a doped polysilicon layer 117, a metal contact 118 and a connector 119 with a high conductivity. The base contact regions 113 stretches down through the base region 109 and into the n-well 104.

The device is covered with an oxide 120 and a PSG (Phosphosilicate Glass) layer.

A trench is thereafter etched outside the semiconductor device region to form a plug 121, being a part of the electrical connection 101. The trench stretches from the PSG layer down to the initially doped substrate, where a plug contact region 122 is created with a high doping of the first type p++. The plug 121 is made of a material with a high conductivity, such as a metal, especially tungsten. The plug is connected, via a connector 123, to any part of the semiconductor device that needs to be grounded, in this case the emitter contact E.

In this way a connection is established from the emitter contact E to a reverse side 124 of the substrate 102, which may be grounded, via the connector 123 and the electrical connection 101, comprising a plug 121 and a plug contact region 122. If a high current is to be led through the established connection, the electrical connection may comprise a plurality of plugs.

Fig. 2a-2e illustrates the manufacturing steps for the semiconductor device including the electrical connection in Fig.1. The figures mainly shows the region where the semiconductor device, in this example a bipolar transistor, is created between the isolation means 105, the plug 121 is located outside this region.

Fig. 2a shows a substrate 102 (p+ type) that has been processed up to a point where the following parts of the process is completed: growing a fist epitaxial layer to form a buried layer 103 (n+ type), growing a second epitaxial layer to form a n-well 104 (n type), introducing isolation means 105, deposition of field oxide 107 with a first and a second opening, creating a highly doped region (n+ type) stretching from the surface 106 of the first opening down to the buried layer 103, creating a base region 109 (p type) at the surface of the second opening, deposition of a polysilicon layer 117 with a high doping of the first type p+ and deposition of a first oxide layer 201 on the polysilicon layer 117. All these steps are performed in a way that are obvious for a person skilled in the art.

Fig. 2b shows a cross section of a semiconductor device where an emitter opening 202 and a collector opening are formed in the first oxide layer 201 and the polysilicon layer 117 down to the base region 109. A second oxide layer 203 is then deposited on top of the semiconductor device.

Fig. 2c shows a cross section of a semiconductor device where the second oxide layer 203 has been etched away leaving only two spacers 204, narrowing the emitter opening. A second polysilicon layer with a high doping of the second type n+ is deposited over the device and, as shown in Fig. 2d, etched to form a polysilicon layer 114 over the emitter opening 202 and a polysilicon layer 125 over the first opening, that is the collector opening. The substrate is subject to an anneal which drives in three regions 112, 113 into the base region 109. The emitter region 112 is formed directly beneath the polysilicon layer in the emitter opening 202 and a base contact region 113 is formed on each side of the emitter region 112 beneath the first polysilicon layer 117, where said base contact regions 113 stretches down through the base region 109 into the n-well 104.

Fig. 2e shows a cross section where metal contacts 111, 115, 118 are created to establish electrical contact to the bipolar transistor 100. This process is well establish and known to a person skilled in the art.

The resulting semiconductor device 100, including the connection from the emitter connection E to the reverse side of the substrate 124, is illustrated and described in Fig. 1.

Figures 1 and 2a-2e only described a NPN bipolar transistor, but naturally can other types of semiconductor devices, such as PNP bipolar transistors, MOS transistors or discrete components, having a ground connection being connected to the reverse side of the substrate as shown in Fig. 1. The semiconductor device may of course be part of a semiconductor circuit, which may consist of a plurality of different semiconductor devices. A major advantage is that a more compact layout of the semiconductor circuit may be obtained, with a reduced number of contact pads.

Fig. 3 shows a perspective view of an integrated circuit 300 comprising a package 302, including pins and contact pads 303, bonding wires 304 and an semiconductor circuit 306, comprising at least one semiconductor device 100 with a ground connection E connected to a ground pin 301 according to the invention.

Each pin, except the ground pin 301, is connected to at least one pad on the semiconductor circuit 306 via the contact pads 303 and the bonding wires 304, respectively. The ground pin 301 is preferably directly connected to a lead frame 305 on which the reverse side 124 of the semiconductor circuit 306 is electrically attached.

A prior art integrated circuit has normally a large number of bonding wires to establish a ground connection from the integrated circuit to the package. The time for making all the connections is dependent on the number of bonding wires to attach. By reducing the number of bonding pads needed, and making the ground connection according to the invention , the procedure for attaching the bonding wires to the bonding pads on the circuit is significantly speeded up due to less bonding wires to attach.

Other ways of electrically connecting the reverse side of the semiconductor circuit may be used, such as connecting the lead frame via at least one separate bonding wire.

Claims

1. A semiconductor device arranged at a surface of a semiconductor substrate, having an initial doping, said device having an electrical connection comprising at least one plug made of a material with a high conductivity, between said initially doped substrate and said surface of the substrate, said device having at least one ground connection arranged to be connected to a ground pin on a package, wherein said at least one ground connection is arranged to be connected to said ground pin using said electrical connection, where said substrate is arranged to be connected to said ground pin via a reverse side of the substrate, opposite said surface, and thereby being arranged to establish a connection between said ground connection and said ground pin.

2. Semiconductor device according to claim 1, wherein , said material is of another type than the substrate.

3. Semiconductor device according to claim 2, wherein said at least one plug is a metal plug.

4. Semiconductor device according to claim 1, wherein said plug extends deeper into the substrate than therein introduced and/or existing PN-junctions.

5. Semiconductor device according to claim 1, wherein the upper end of each plug is connected to said ground connection via an electrically conductive material, especially a material with a high conductivity, especially a metal material.

6. Semiconductor device according to claim 1, wherein said semiconductor device is a high frequency device.

7. Semiconductor device according to claim 6, wherein said device is a power device.

8. Semiconductor device according to claim 6, wherein said device is a bipolar transistor and said ground connection is an emitter connection.

9. Semiconductor device according to claim 6, wherein said transistor is a MOS transistor and said ground connection is a source connection.

10. A semiconductor integrated circuit mounted in a package, said package having a plurality of pins connecting to the semiconductor circuit, and said circuit having a plurality of semiconductor devices, wherein at least one of said semiconductor devices is a semiconductor device according to claim 1.

Abstract

The present invention relates to a semiconductor device arranged at a surface of a semiconductor substrate having an initial doping having an electrical connection comprising at least one plug made of a material with a high conductivity, especially a material other than the substrate, especially a metal plug, between said initially doped substrate and said surface of the substrate. The device has at least one ground connection arranged to be connected to a ground pin on a package. The ground connection is arranged to be connected to said ground pin using said electrical connection, where the initially doped substrate is arranged to be connected to said ground pin via a reverse side of the substrate, opposite said surface, and thereby being arranged to establish a connection between said ground connection and said ground pin.

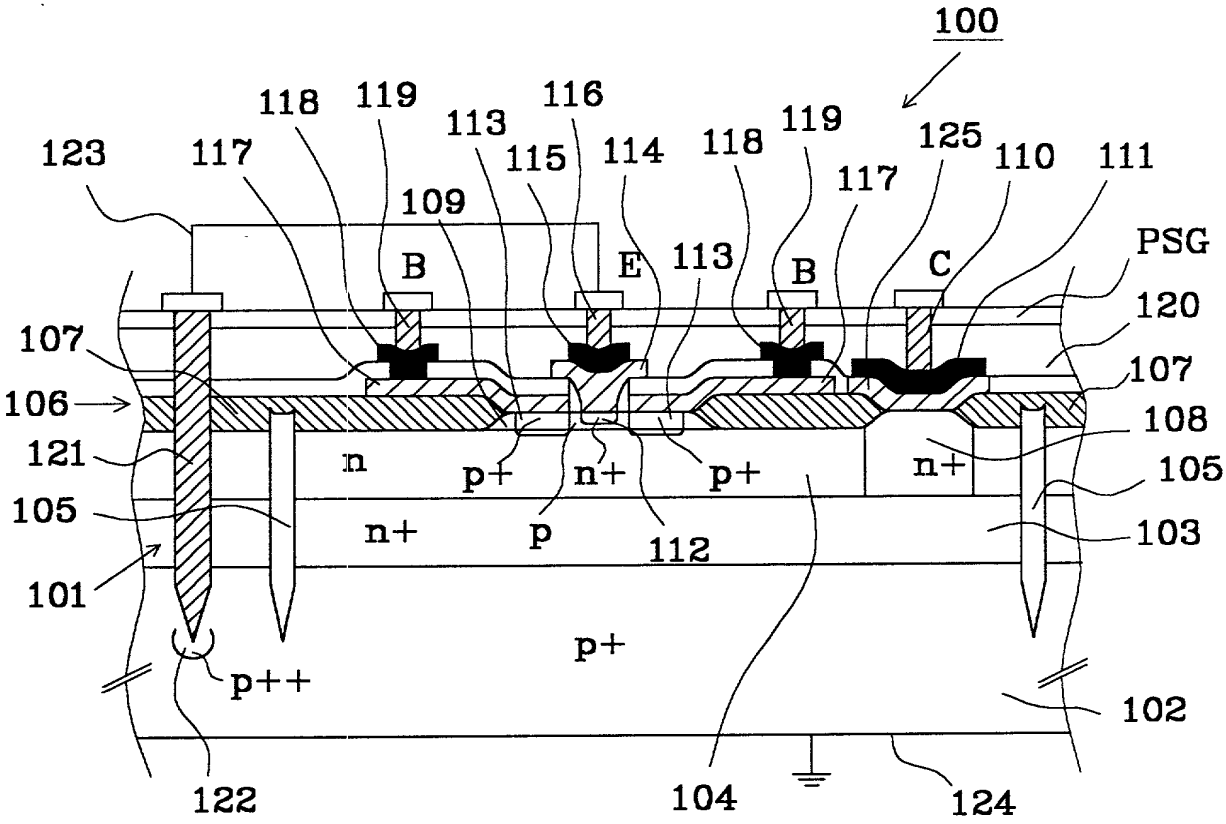

100
123
117
118
119
113
116
115
114
118
119
117
125
110
111
109
B
E
113
B
C
PSG
120
107
106
121
105
101
n
p+
n+
p+
n+
108
105
n+
p
112
103
p+
p++
102
122
104
124

Fig. 1

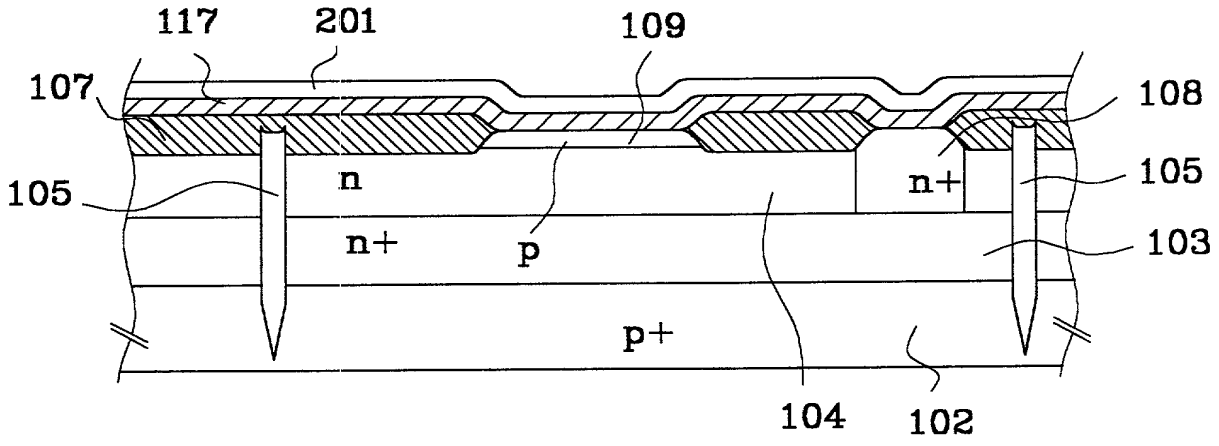
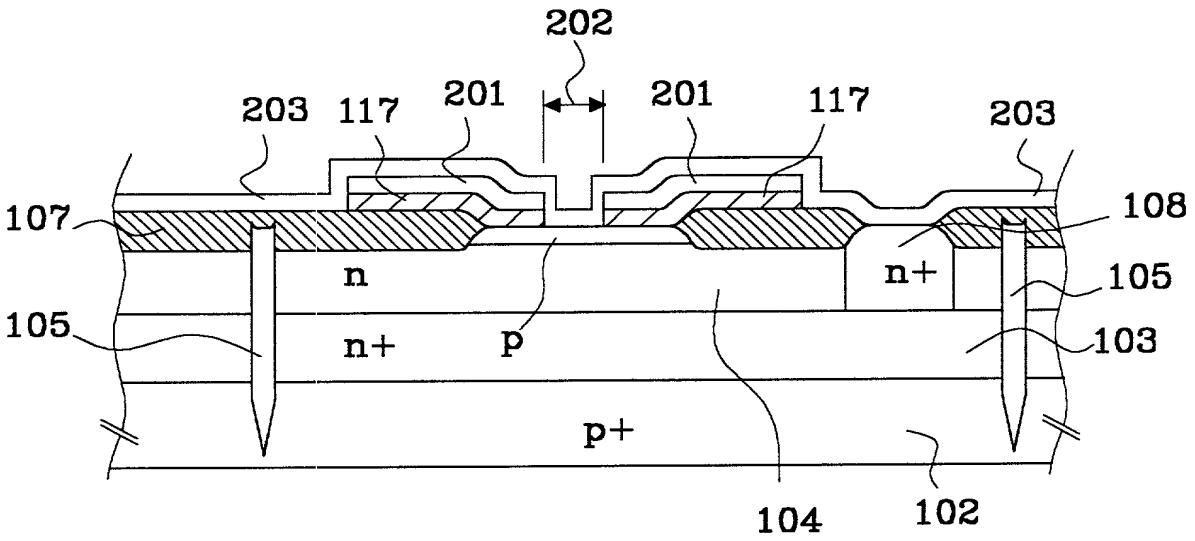

117
201
109
107
108
105
n
n+
105
n+
p
103
p+
104
102

Fig.2a


202
203
117
201
201
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107
108
n
n+
105
105
n+
p
103
p+
104
102

Fig. 2b

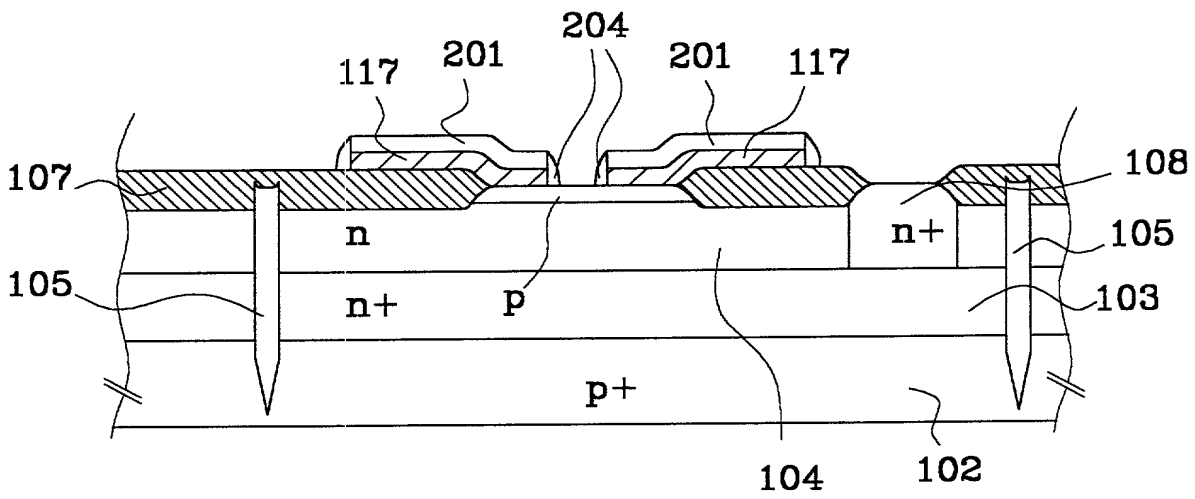
204
117
201
201
117
107
108
n
n+
105
105
n+
p
103
p+
104
102

Fig. 2c

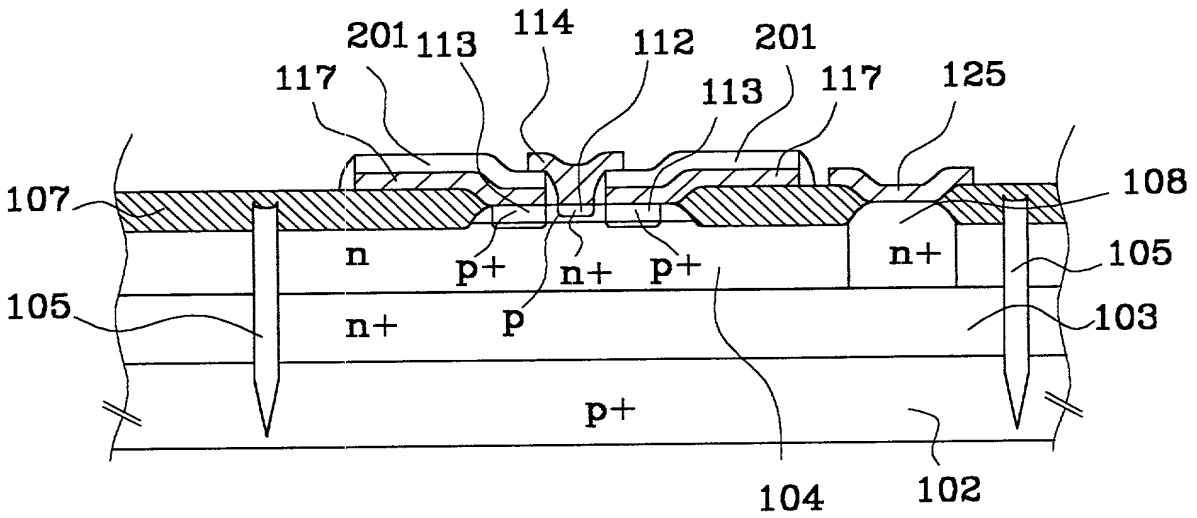
201
113
114
112
201
117
113
117
125
107
108
n
p+
n+
p+
n+
105
105
n+
p
103
p+
104
102

Fig. 2d

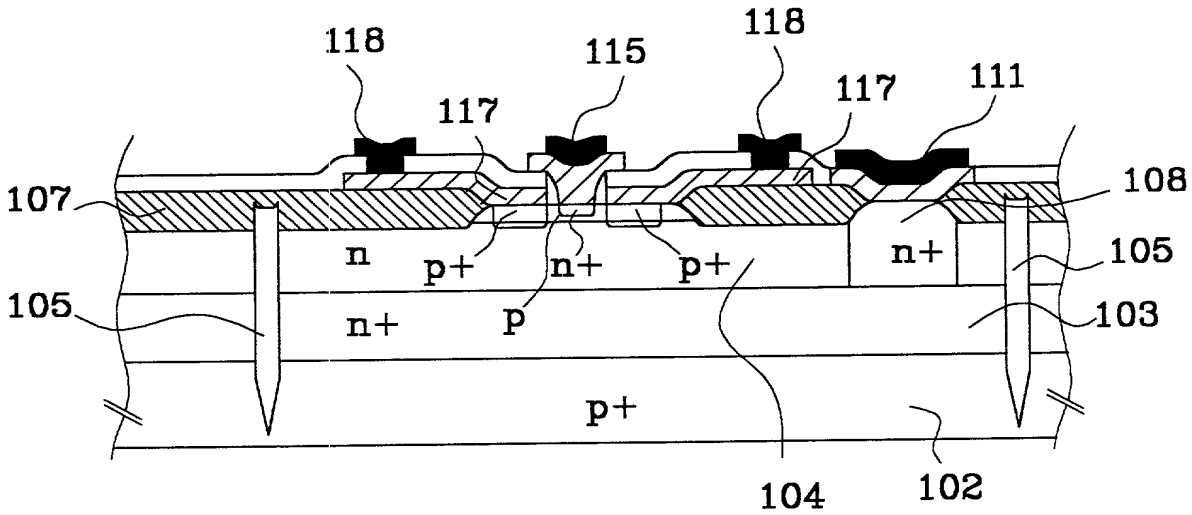
118
115
118
117
117
111
107
108
n
p+
n+
p+
n+
105
105
n+
p
103
p+
104
102

Fig. 2e

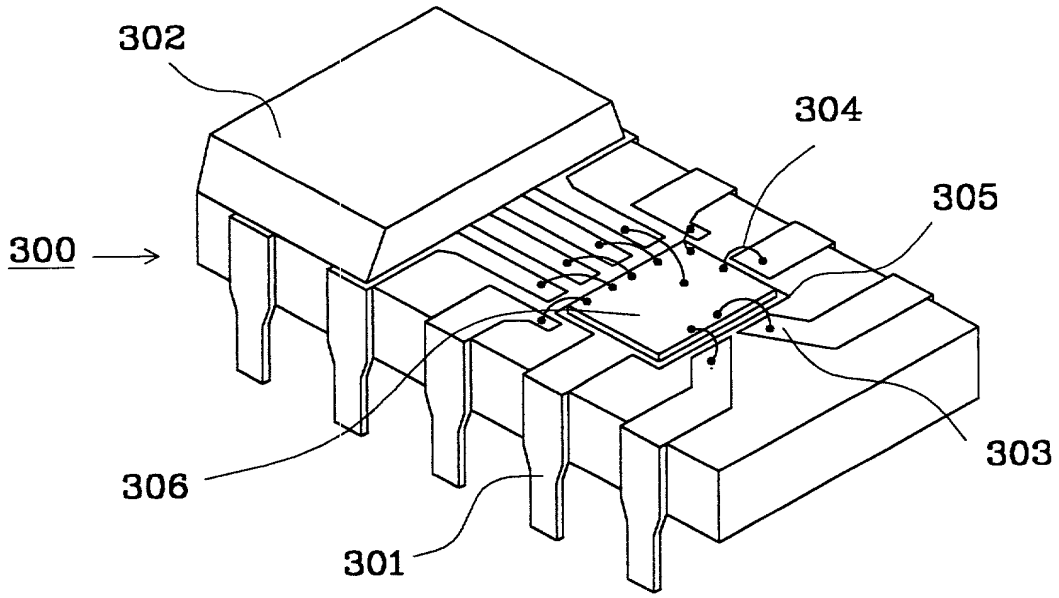

Fig. 3

COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION	Attorney's Docket No. 032840-003

As a below-named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (if only one name is listed below) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (if more than one name is listed below) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

SEMICONDUCTOR DEVICE WITH DEEP SUBSTRATE CONTACTS

the specification of which

(check one) ☒ is attached hereto;

☐ was filed on _____ as

Application No. _____

and was amended on _____; (if applicable)

I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE;

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than twelve months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 and/or Sec. 365 of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application(s) on which priority is claimed:

COMBINED DECLARATION AND POWER OF ATTORNEY	Attorney's Docket No. 032840-003

COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
Sweden	9900446-7	10 February 1999	YES X NO_
			YES_ NO_

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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COMBINED DECLARATION AND POWER OF ATTORNEY	Attorney's Docket No. 032840-003

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POST OFFICE ADDRESS		
FULL NAME OF FIFTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF SIXTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF SEVENTH JOINT INVENTOR. IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF EIGHTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF NINTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	
POST OFFICE ADDRESS		
FULL NAME OF TENTH JOINT INVENTOR, IF ANY	SIGNATURE	DATE
RESIDENCE	CITIZENSHIP	